WHAT IS CLAIMED IS:

1. A filter circuit comprising:

a first differential transistor pair biased by a first differential input;

a second differential transistor pair biased by a second differential input, the second input having been received prior to the first differential input;

at least one current source coupled to provide tail currents for the differential pairs;

wherein the transistors which are biased by present and previous inverted inputs have a first output terminal; and

wherein the transistors which are biased by present and previous non-inverted inputs have a second output terminal.

2. The filter circuit of claim 1, wherein the output nodes are coupled to at least one load selected from the group consisting of a regenerative latch, a passive load, an active filter, and an amplifier.

3. The filter circuit of claim 1, wherein the tail current of the first differential pair is different than the tail current of the second differential pair.

4. The filter circuit of claim 3, wherein the tail currents are provided by a plurality of variably controlled current sources.

5. The filter circuit of claim 3, wherein the tail current differential is provided by a difference in channel widths between the first and second transistor pairs.

6. The filter circuit of claim 1, further comprising first and second offset-inducing differential pairs connected in parallel to the first and second differential pairs, respectively.

7. The filter circuit of claim 6, wherein the channel widths of the transistors in each differential pair are not equal and wherein the difference in channel width in the offset-inducing differential pairs is opposite that of the first and second differential pairs.

8. The filter circuit of claim 7, wherein the tail currents for the first and second offset-inducing differential pairs are equally and oppositely offset from a nominal current level relative to the tail current for the first or second differential pairs, respectively.

9. The amplifier circuit of claim 8, wherein the output nodes provide an amplified, offset and filtered differential signal.

10. The filter circuit of claim 1, wherein the transistors of the differential pairs are p-channel MOSFET transistors.

11. The filter circuit of claim 1, wherein the output nodes provide an amplified, offset and filtered differential signal.

12. The filter circuit of claim 1, further comprising a third differential pair being biased by a third differential input received after the first differential input, the transistor which is biased by an inverted input being coupled to the first output node and the transistor which is biased by a non-inverted input being coupled to the second output node.

13. The filter circuit of claim 1, wherein the output nodes are connected to an input of another circuit element.

14. A filtering method comprising:

receiving first and second differential inputs, the second input having been received prior to the first input;

biasing the first and second differential input pairs with the first and second differential inputs, respectively;

weighting the first and second differential inputs by modulating the gain of at least one of the differential input pairs;

tapping the first and second output nodes to obtain a filtered signal, wherein the first and second output nodes are connected to the transistors which are biased by the inverted inputs and non-inverted inputs, respectively.

15. The method of claim 14, wherein the output nodes are coupled to at least one load selected from the group consisting of a regenerative latch, a passive load, an active filter, and an amplifier.

16. The method of claim 14, wherein the gain is modulated by altering the tail currents of the differential pairs.

17. The method of claim 14, wherein the gain is modulated by altering the tail currents provided by a plurality of variably controlled current sources.

18. The method of claim 14, wherein the gain is modulated by altering the widths of the channels of the transistors.

19. The method of claim 14, further comprising inducing an offset by connecting first and second offset-inducing differential pairs in parallel to the first and second differential pairs, wherein the channel widths in at least one transistor pair are mismatched.

20. The method of claim 19, further comprising inducing an offset in a third differential input, the third differential input having been received after the first signal.

21. The method of claim 19, further comprising equally and oppositely offsetting the tail currents of the first and second offset-inducing differential pairs from a nominal current level relative to the tail current for the first or second differential pairs, respectively.

22. The method circuit of claim 14, wherein the filtered signal is also amplified and offset.

23. The method of claim 14, wherein the transistors of the differential pairs are n-channel MOSFET transistors.

24. The method of claim 14, further comprising receiving a third differential signal, the third signal having been received after the first signal, biasing a differential input pair with the third signal, and weighting the third signal by modulating the gain of at least one of the differential input pairs.

25. A communications system comprising:

(a) a transmitter producing a differential voltage signal;

(b) a receiver comprising:

(1) a sample-and-hold circuit that receives the differential voltage signal and samples and holds values of the differential voltage signal; and

(2) a filter circuit comprising:

a first differential transistor pair biased by a first differential input;

a second differential transistor pair biased by a second differential input, the second input having been received prior to the first differential input;

at least one current source coupled to provide tail currents for the differential pairs;

wherein the transistors which are biased by present and previous inverted inputs have a first output terminal; and

wherein the transistors which are biased by present and previous non-inverted inputs have a second output terminal.

26. The communications system of claim 25, wherein the transmitter and the receiver reside on different circuit boards.

27. The communications system of claim 25, wherein the transmitter and the receiver reside on different integrated circuit die.

28. The communications system of claim 25, wherein the filter further comprises first and second offset-inducing

differential pairs connected in parallel to the first and second differential pairs, respectively, wherein the channel widths of the transistors in each differential pair are not equal and wherein the difference in channel width in the offset-inducing differential pairs is opposite that of the first and second differential pairs.